REMARKS

Claims 1-30 are currently in the application.

Claim Objections

In response to the Examiner's claim objections, we have amended claims 2-3 and 14-19 as suggested. We have also amended claims 4-7, 9, and 11 to 16 and 18 in response to the Examiner's substantive objection under 35 USC § 103. We submit that the amendments to those claims are fully responsive to the Examiner's objection to claims 9 and 18.

Claim Rejections

The Examiner has rejected claims 1-3 as being anticipated by Schzukin (US 6,442,747) and has referred to specific passages of the Schzukin patent which are alleged to disclose the method of the present application. However, we respectfully submit that, whilst the Schzukin patent relates to similar technology in that it too discloses a method of synthesizing a CRC generator circuit, it fails to disclose a method in which a hardware description language (HDL), such as VHDL, is used to build code directly describing synthesizable logic for performing polynomial division.

With respect, the Examiner cites passages from Schzukin which refer to use of HDL to build code describing synthesizable logic. However, this method is not performed using the hardware description language directly. Rather, Schzukin teaches an optimization method which functions to reduce the gate count and complexity of the resulting circuit as well as reduce the delay. This is achieved by firstly preparing optimized polynomial-specific equations and subsequently translating these into HDL code which in Schzukin's case is VHDL code. Thus the HDL code disclosed in Schzukin is indirectly generated as the last step in Schzukin's process by a code generator. Hence

the HDL or VHDL code that is generated through Schzukin's process is generated on a case-by-case basis and is not generic HDL code.

The optimization method disclosed in Schzukin operates iteratively, generating remainder equations for a CRC generator, given a specific generator polynomial. During each iteration duplicate terms in each remainder term are removed (or replaced with a zero). Once all the duplicate terms in the remainder equations are removed, the equations are sorted and rebuilt and then translated into a hardware description language such as VHDL. The VHDL code is not built directly describing the generator circuit. The resulting VHDL code is then synthesized to build a CRC generator circuit. Thus, the objectives of the Schzukin method are to create a CRC circuit implementation having a smaller area and lower delay than the prior art approaches.

In contrast, the present application aims to simplify the code building process which is associated with the prior art approaches to building CRC generators, by obviating the complex optimization method of Schzukin, and using generic HDL code such as VHDL to describe the logic required for performing the polynomial division in a generic and direct fashion. Thus, the present invention has an advantage over Schzukin in that the HDL code is generic, being applicable to any generator polynomial and bus-width combination hence eliminating the requirement to generate new HDL or VHDL code for every unique polynomial and bus-width combination. To clarify this aspect of the invention, we respectfully request amendment of claim 1 as shown in the preceding pages to include the word generic. Basis is provided in the description on page 6 at lines 28 to 30.

Whilst in various embodiments the present invention may also result in a reduction in the gate count and complexity of the resulting CRC generator circuit, the present invention has the added special advantage that it eliminates the need to use a code generator or translator to translate the CRC generator equations (which result from the optimization method of Schzukin) into HDL code. The circuit designer of the present invention does not use a code generator to generate HDL code. Rather, in the designer uses P (the CRC polynomial) and B (the data-bus width) as inputs to generic HDL code

which has been created to describe the behavior or structure of the CRC calculating device.

The generic HDL code of the present invention describes the structure or behavior of the generator circuit independently of the specific CRC generator polynomial or the data-bus width combination for which the CRC generator circuit is being built. This is in direct contrast with the method of Schzukin which optimizes code for CRC generators on a case-by-case basis, and is dependent on the specific generator polynomial, G(x) (a parameter of the optimization method) and data-bus width (which determines the number of iterations of the method).

We therefore submit that claim 1 is not anticipated by Schzukin. Since claims 2-3 are dependent on claim 1, we also submit that claims 2-3 are not anticipated by Schzukin.

The Examiner has also rejected claims 1-3 as being anticipated by Gallezot (US 2002/0144208). We respectfully disagree with the Examiner's rejection of claim 1 in the light of Gallezot for the following reasons.

The Abstract does make reference to automatic generation of the logic necessary to carry out a CRC calculation. However, Gallezot does not anywhere disclose use of HDL code to build generic code directly describing synthesizable logic for performing a polynomial division. Whilst Gallezot does refer on page 5 at paragraph 71 to use of HDL code for synthesizing logic, this is in the context of the method of the invention described in Gallezot and in particular, the method of Figures 12 and 13.

The methods of Figures 12 and 13 respectively relate to forward and backward computation of CRCs. This methodology is complex and does, in itself, not relate to the issues presently under consideration. However, the methods disclosed in Gallezot with reference to Figures 12 and 13 result in recordal of vectors. When enough vectors have been recorded, they are eventually used for synthesizing the corresponding logic of XOR's but the Gallezot method does not use HDL directly describing the necessary logic.

Moreover, Gallezot indicates that the inventive method is to be used "so as to obtain the logic, corresponding to a CRC and a particular generator polynomial, to allow computation N-bit at a time". The automatic logic generation method put forth in Gallezot must be preceded by translation of the vectors which result from Gallezot's CRC calculating method into HDL, and this must occur on a case-by-case basis for each specific generator polynomial for which a generator circuit is required. Therefore, Gallezot does not disclose or teach use of Hardware Description Language directly building generic code capable of receiving as a parameter any generator polynomial.

In the light of the above, we respectfully submit that claim 1, as amended, is not anticipated by Gallezot. Since claims 2-3 are dependent on claim 1, we respectfully submit that they too are novel over Gallezot.

The Examiner has also objected under 35 USC § 103 that claims 4-6 and 11-15 are unpatentable over Gallezot (US 2002/0144208) in view of Schzukin (US 6,442,747). In response, we have deleted claims 4-6 and 13-15 and amended claims 7, 9, 11-12 and claims 16 and 18 .

Claim 7 has been rewritten in independent form as recommended by the Examiner, incorporating all the features of original claim 4. Claims 9, and 11-12 have been amended to depend from claim 7. New claim 21 recites the subject matter of original claim 5, but depends from currently amended claim 7.

Similarly, claim 16 has been rewritten in independent form as recommended by the Examiner, incorporating all the features of original claim 13. Claim 18 has been amended to depend from claim 16.

New Claim 20 recites the subject matter of original claim 14, rewritten to depend from amended claim 16.

New claim 21 corresponds to original claim 18, rewritten in independent form as recommended by the Examiner, incorporating all the features of original claim 13. New

claims 22-25 correspond to original claims 19, 16, 17 and 14 respectively, rewritten to depend from new claim 21.

New claim 26 recites the subject matter of original claim 9, rewritten to incorporate all the features of original base claim 4. New claims 27-30 correspond to original claims 10, 7, 8 and 5 respectively, rewritten to depend from new claim 26.

We respectfully submit that amended and new claims 4-30 fall within the scope of allowable subject matter as identified by the Examiner, and submit that presently amended claims 1-30 are patentable over Schzukin and Gallezot when taken separately under 35 USC § 102 and when combined under 35 USC § 103.

Applicant respectfully submits that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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